Instructions on Placement and Routing by Encounter

1. Go to "run_dir" folder, source /etc/software/edi
   Type "encounter" to start.

2. In the command window, type "set rda_Input(ui_pwrnet) {VDD}" and "set rda_Input(ui_gndnet) {VSS}". By using these 2 commands, we set two nets VDD and VSS.

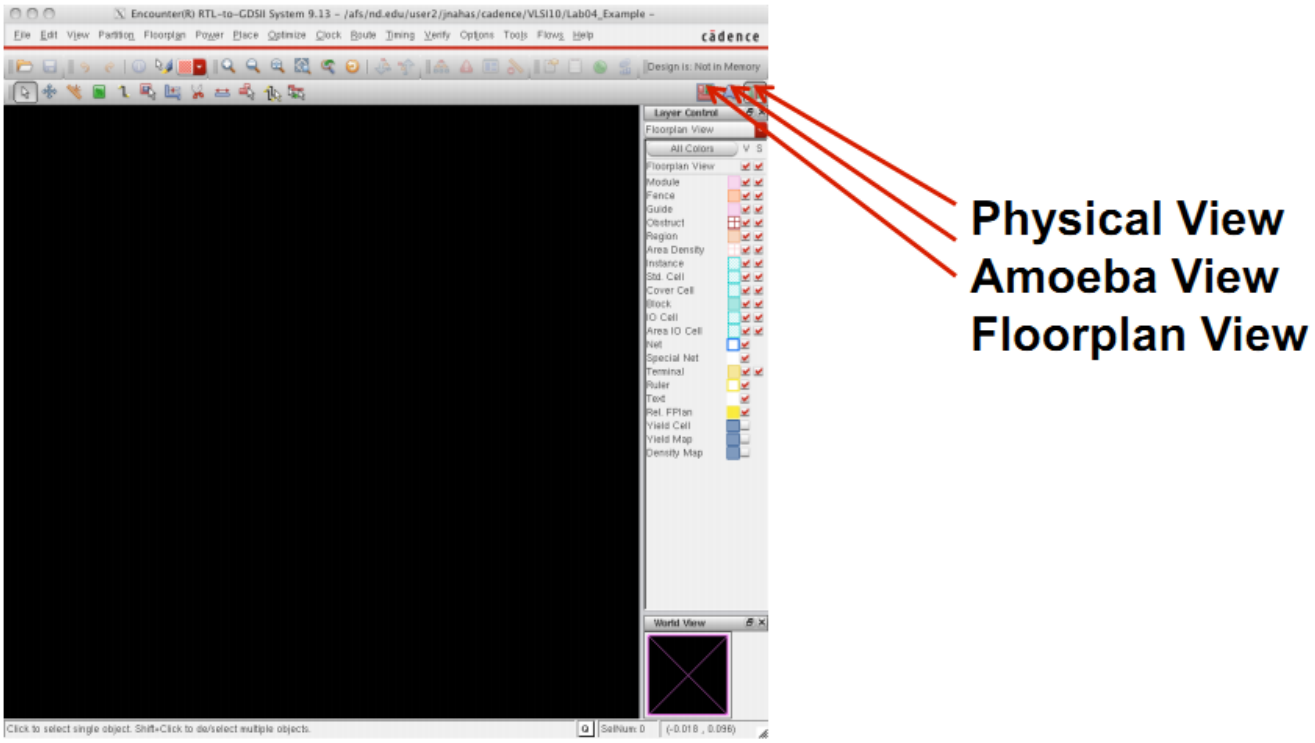
3. Select File→Import RTL

   In the "Logical" tab:
   - Set "Verilog Files" to your synthesis result of Lab 4. It should be in "rc/syn/run_dir" of your Lab 4 directory. *Please double-click the file to select.*
   - For "Top Level", select "Auto Assign".
   - Set "Max Libs" to the "tcbn65gpluswc.lib", which is located in "encounter/libdir/lib" folder.
   - Set "Constraint Files" to the .sdc file which is generated in your Lab 4 and should be located in "rc/syn/run_dir" directory of your Lab 4. It describes the constraint settings of your Lab 4. The RTL compiler outputted them as a file for Encounter to use.

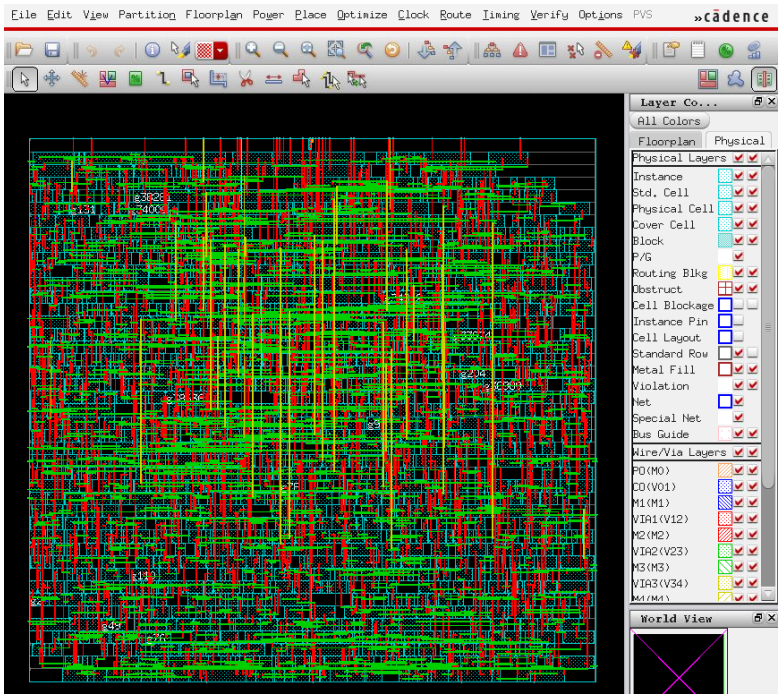
   In the "Physical" tab:
   1. Set "LEF Files" to "tcbn65gplus_8lmT2.lef", which is located in "encounter/libdir/lef". It contains the geometry information of the standard cells, which is needed during placement and routing.

   Click "OK" to submit. Now, we finished specifying the inputs for placement and routing.

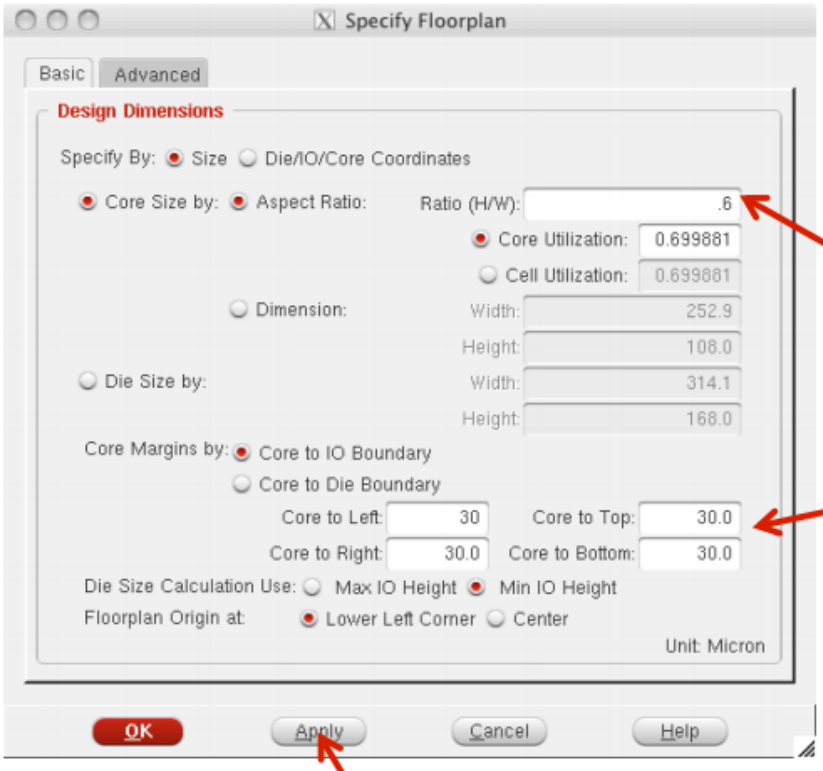
4. Select File→RTL Synthesis
   Select "Proceed with Placement", and then click "OK". Ignore the warning about not specifying floorplan or def file.



Now, please select the physical view to display your layout. You may need to press "F" to see the whole circuit.



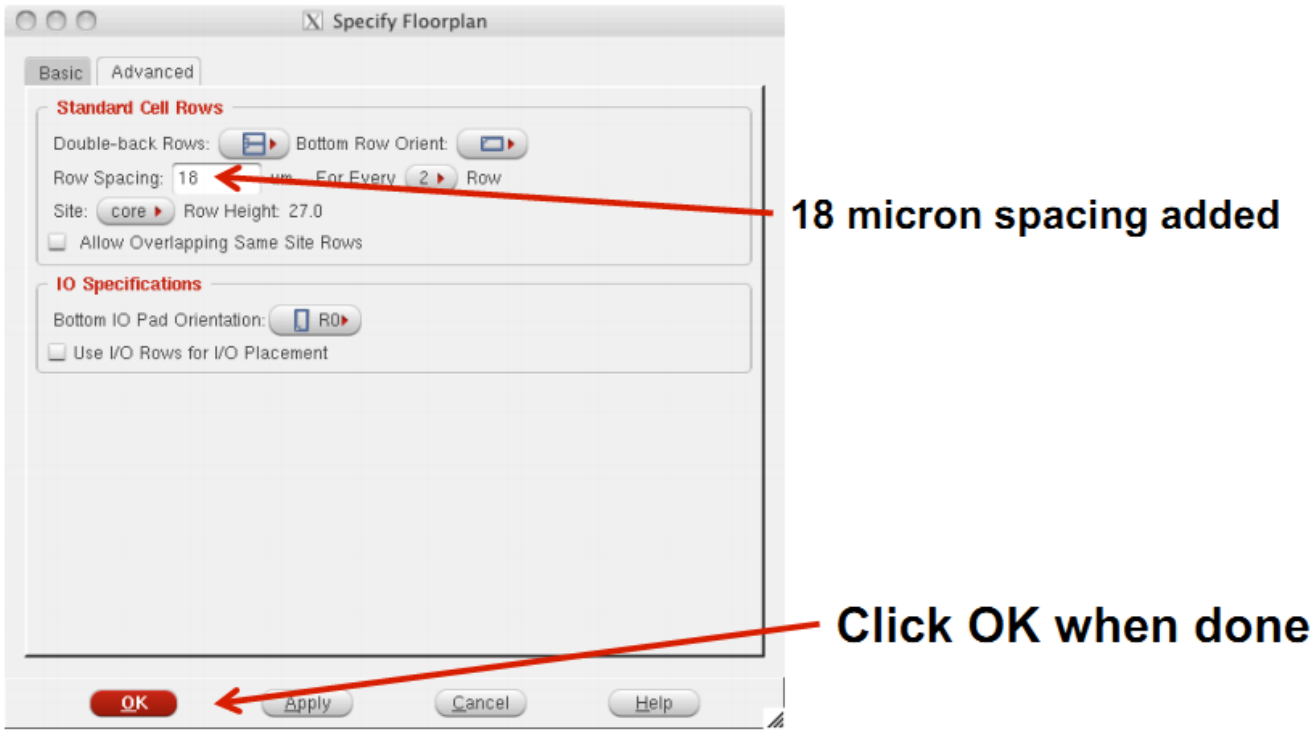
5. Select Floorplan→Specify Floorplan
   Set the parameters and options for both "Basic" and "Advanced" tabs using the values as shown in the figures below. Please note that these parameters will affect your layout result.



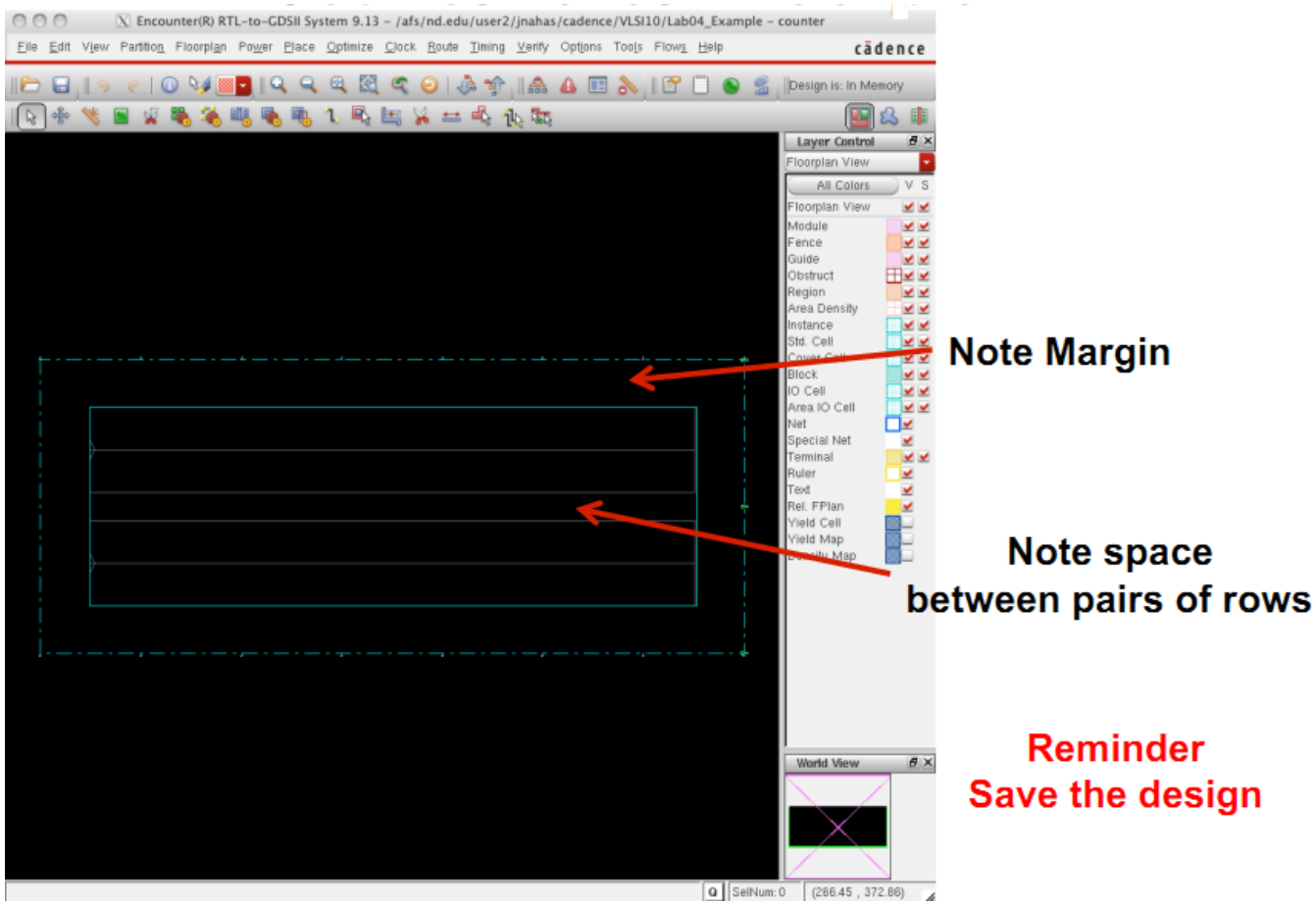
Aspect Ratio Can be adjusted if desired

30 micron margins added
Left
Right
Top
Bottom

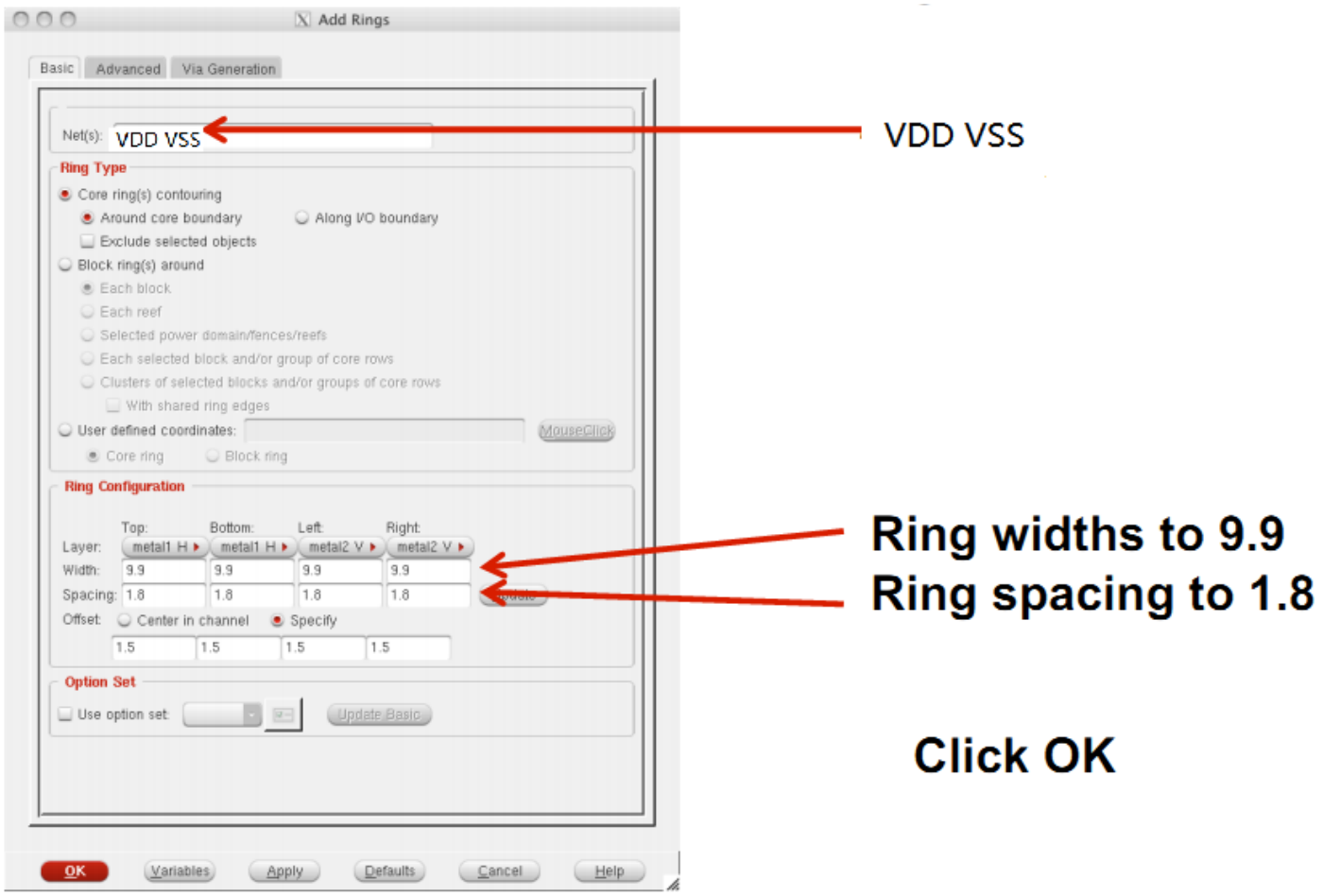
Click Apply to see how floorplan changes affect layout on main screen



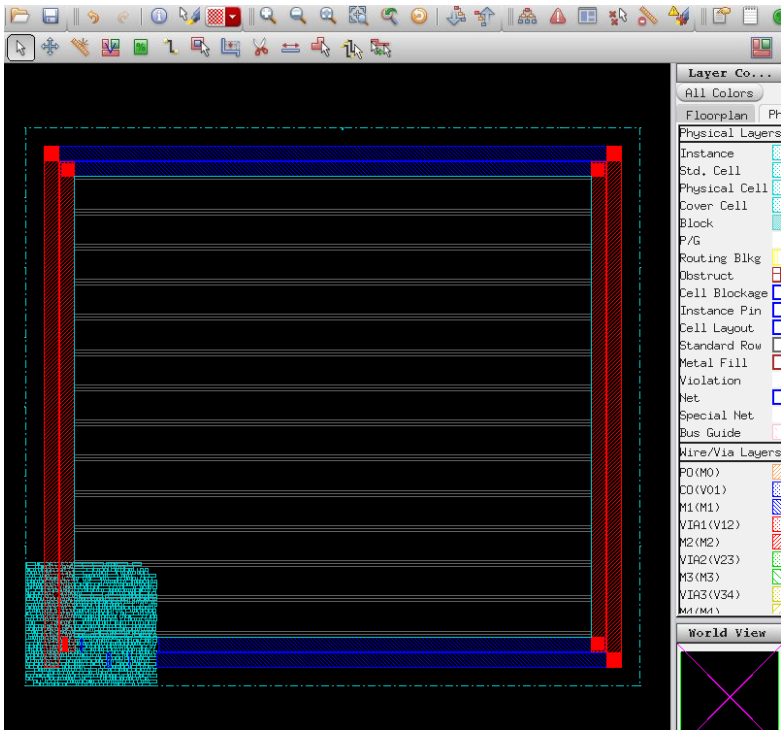
Then the placement region will be displayed:



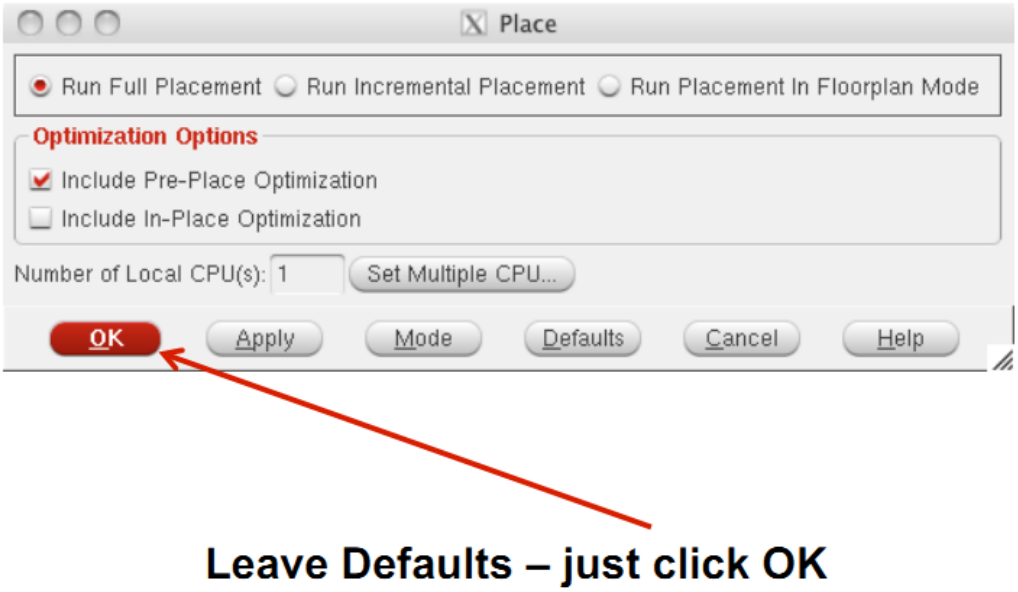
6. Select Power→Power Planning→Add Ring
   Set the parameters and options for "Basic" tab using the values as shown in the figure below.



Then the power rings will be displayed:

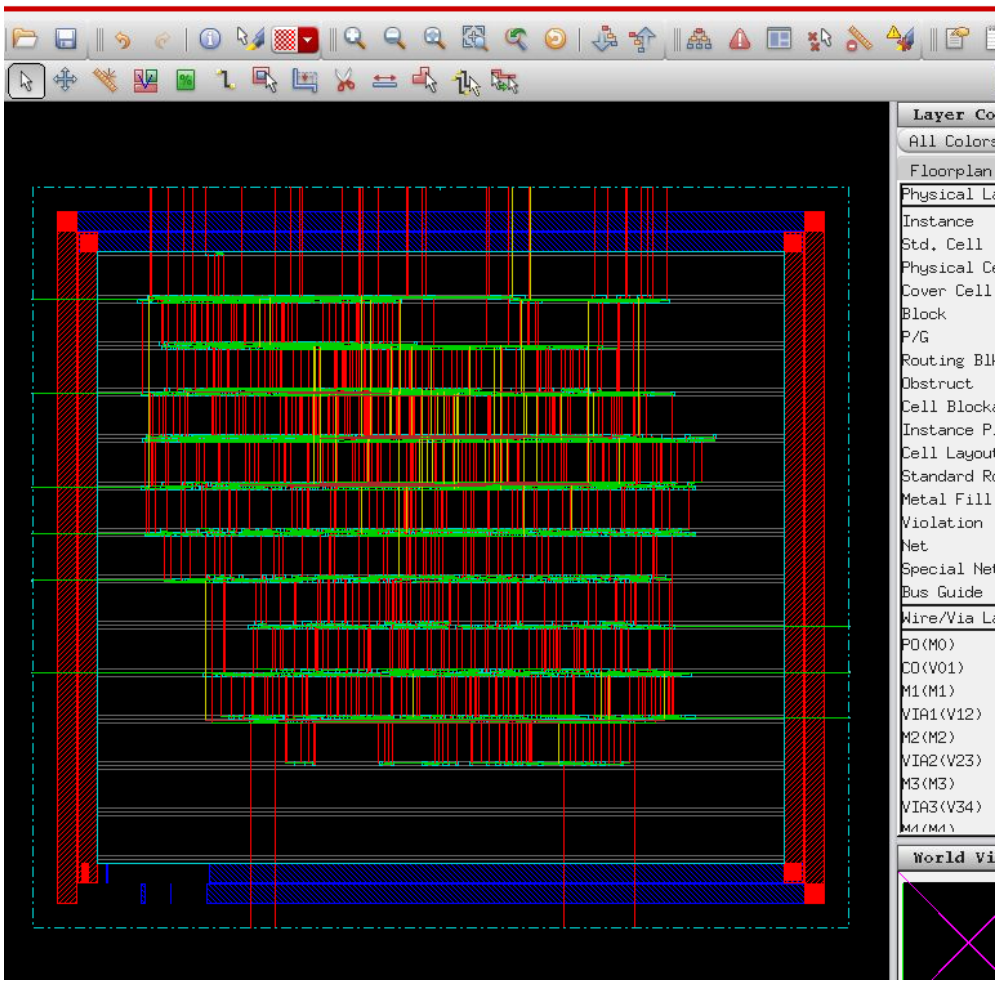


7. Select Place→Place Standard Cell
   Set the options as shown in the figure below.

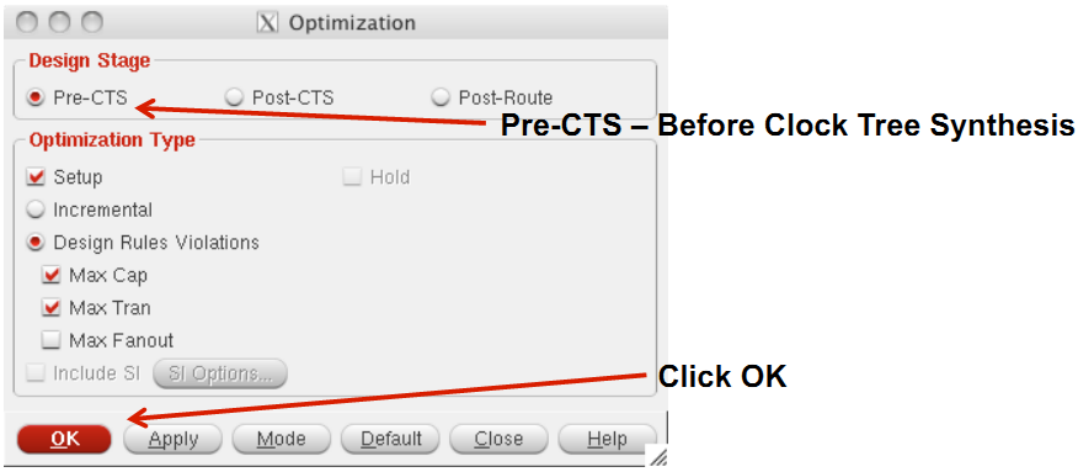


Leave Defaults – just click OK

You may need to press "F" again to view the whole circuit.



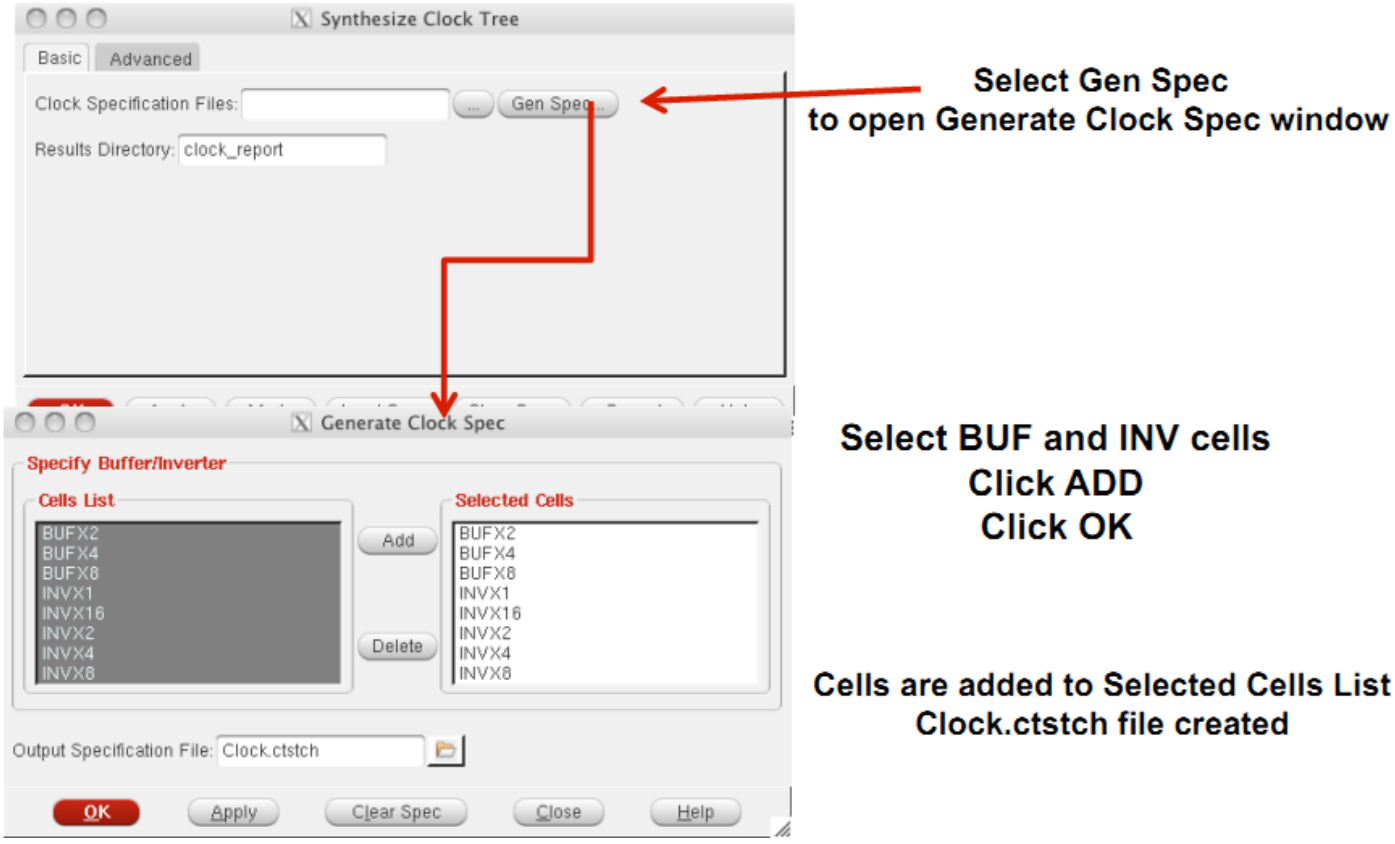
8. Select Optimize→Optimize Design
   Set the options as shown in the figure below.

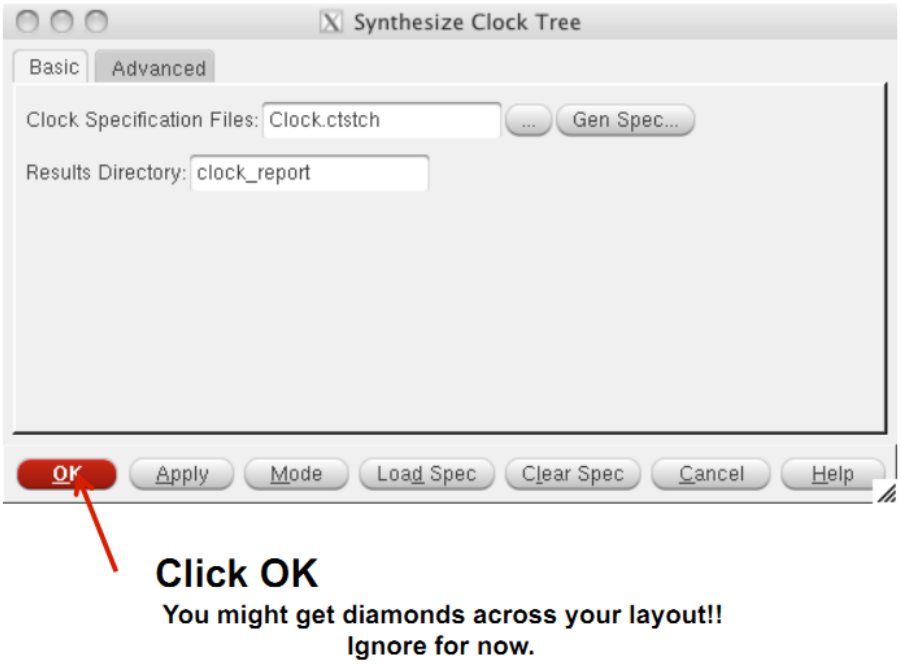


Note: You might get an error message
Ignore for now.

"CTS" means clock tree synthesis. Pre-CTS means before clock tree synthesis. In here, please note that we have selected the option to correct setup time violations.

9. Select Clock→Synthesize Clock Tree
   Set the options as shown in the figures below.





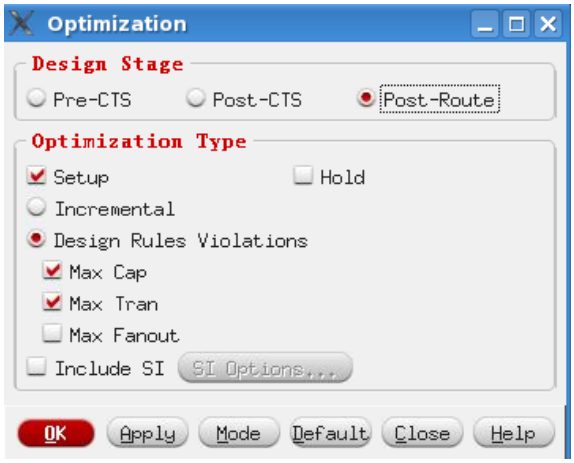
You can view the clock tree by selecting Clock→Display→Display Clock Tree.

10. Select Optimize→Optimize Design again
    Set the options as shown in the figure below.

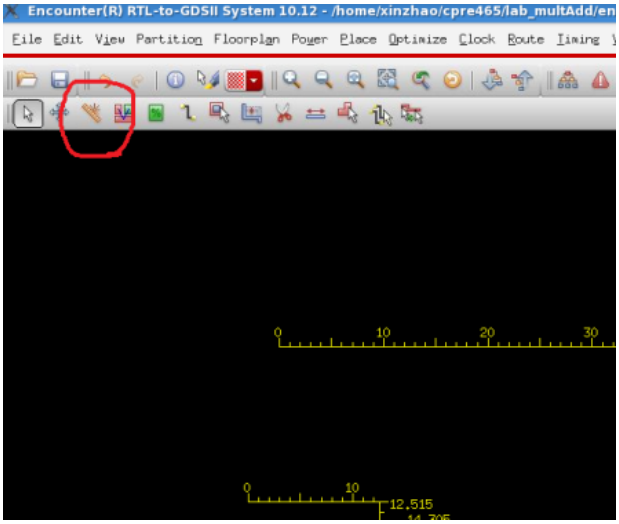
We selected Post-CTS this time. It means the optimization is performed after clock tree synthesis.

11. Select Route→NanoRoute→Route
    Set the parameters and options as shown in the figure below.

12. Select Optimize→Optimize Design
    This time, we select Post-Route because we have already performed routing.



13. Now you have finished placement and routing.
    - To report power, type report_power.
    - To get area information, use the ruler which is circled by red below:



    - To report worst timing path, type report_timing in the command window.
    - To debug timing violations, select Timing→Debug Timing.
    - To save your design, type "saveNetlist -excludeLeafCell design_pr.v" in the command window.
    - To output RC parameters of your design, type "rcOut -spef design.spef" in the command window.
    - To output .sdf (Standard Delay Format) file, select Timing→Write SDF. The .sdf file contains the information required for signal delay calculation. This file would be needed if we perform post layout simulation in ModelSim.