Instructions on Placement and Routing by Encounter

- 1. Go to "run_dir" folder, source /etc/software/edi Type "encounter" to start.
- 2. In the command window, type "set rda_Input(ui_pwrnet) {VDD}" and "set rda_Input(ui_gndnet) {VSS}". By using these 2 commands, we set two nets VDD and VSS.
- 3. Select File→Import RTL

In the "Logical" tab:

- Set "Verilog Files" to your synthesis result of Lab 4. It should be in "rc/syn/run_dir" of your Lab 4 directory. *Please double-click the file to select*.
- For "Top Level", select "Auto Assign".
- Set "Max Libs" to the "tcbn65gpluswc.lib", which is located in "encounter/libdir/lib" folder.
- Set "Constraint Files" to the .sdc file which is generated in your Lab 4 and should be located in "rc/syn/run_dir" directory of your Lab 4. It describes the constraint settings of your Lab 4. The RTL compiler outputted them as a file for Encounter to use.

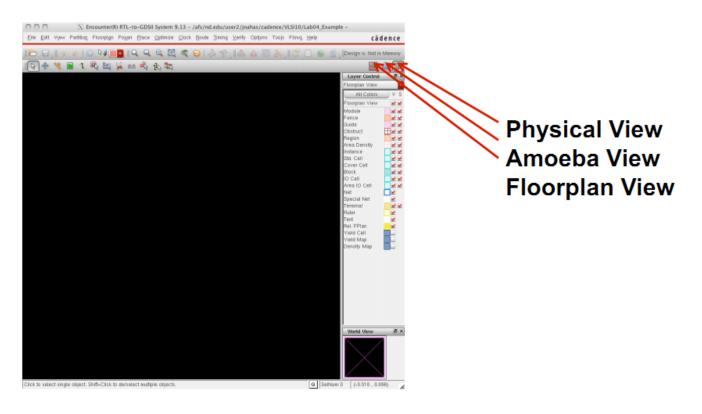
In the "Physical" tab:

1. Set "LEF Files" to "tcbn65gplus_8lmT2.lef", which is located in "encounter/libdir/lef". It contains the geometry information of the standard cells, which is needed during placement and routing.

Click "OK" to submit. Now, we finished specifying the inputs for placement and routing.

4. Select File \rightarrow RTL Synthesis

Select "Proceed with Placement", and then click "OK". Ignore the warning about not specifying floorplan or def file.



Now, please select the physical view to display your layout. You may need to press "F" to see the whole circuit.

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5. Select Floorplan→Specify Floorplan

Set the parameters and options for both "Basic" and "Advanced" tabs using the values as shown in the figures below. Please note that these parameters will affect your layout result.

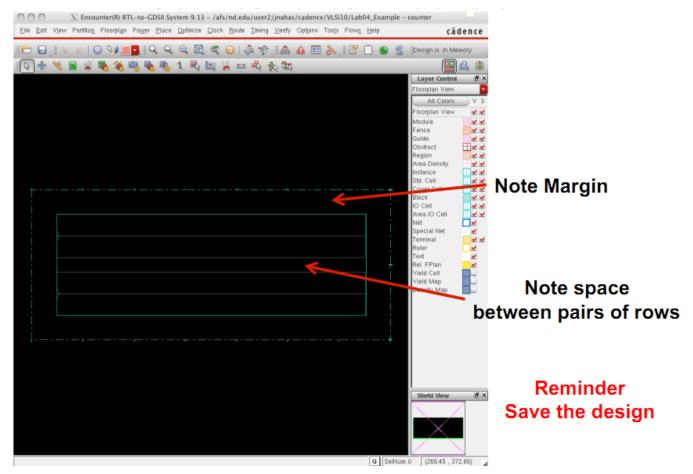
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	Cell Utilization:	0.699881	Can be adjusted
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	Height:	168.0	30 micron
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Core to Right:	30.0 Core to Bottom:	30.0	
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			Bottom
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Click Apply to see how floorplan changes affect layout on main screen

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000	X Specify Floorplan		
Basic Advanced			
Standard Cell Rows			
Double-back Rows:	Bottom Row Orient: 🗾 🕨		
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Site: core Row Height:			18 micron spacing added
Allow Overlapping Same	Site Rows		
10 Specifications			
Bottom IO Pad Orientation:			
Use I/O Rows for I/O Place	ement		
			Click OK when done
<u>o</u> k ←	Apply <u>C</u> ancel	Help	4

Then the placement region will be displayed:



6. Select Power → Power Planning → Add Ring

Set the parameters and options for "Basic" tab using the values as shown in the figure below.

VDD VSS
VDD VSS
VDD VSS
Ding widths to 0.0
Ring widths to 9.9
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——— Ring spacing to 1.3
Click OK

Then the power rings will be displayed:

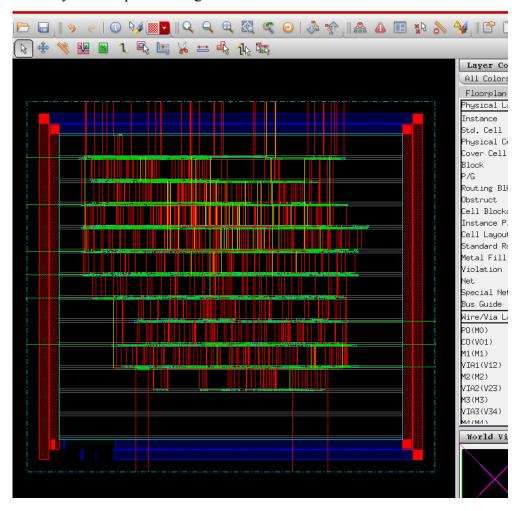
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7. Select Place \rightarrow Place Standard Cell

Set the options as shown in the figure below.

000	X Place
🖲 Run Full Placeme	t 🔾 Run Incremental Placement 🔾 Run Placement In Floorplan Mode
- Optimization Option	
✓ Include Pre-Place ☐ Include In-Place	
Number of Local CPU(): 1 Set Multiple CPU
	pply <u>M</u> ode <u>D</u> efaults <u>C</u> ancel <u>H</u> elp
Le	ave Defaults – just click OK

You may need to press "F" again to view the whole circuit.



8. Select Optimize → Optimize Design

Set the options as shown in the figure below.

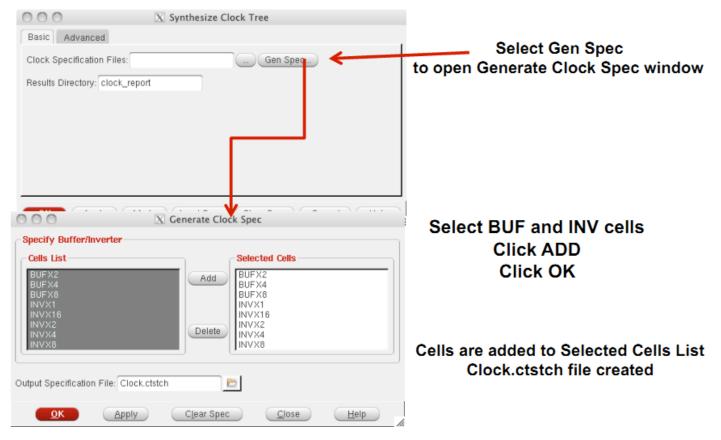
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Optimization Type	9	Pre-CTS	 Before Clock Tree Synthesis
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🗌 Include SI 💽	Options)		 Click OK
	y <u>M</u> ode <u>D</u> e	fault <u>C</u> lose <u>H</u> elp	

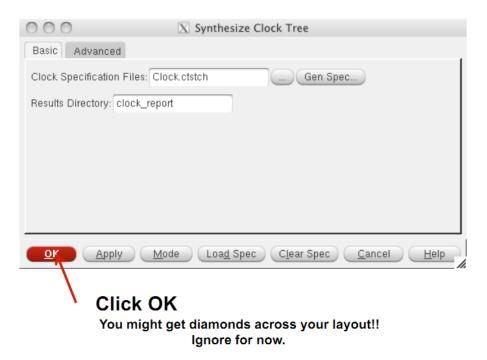
Note: You might get an error message Ignore for now.

"CTS" means clock tree synthesis. Pre-CTS means before clock tree synthesis. In here, please note that we have selected the option to correct setup time violations.

9. Select Clock \rightarrow Synthesize Clock Tree

Set the options as shown in the figures below.





You can view the clock tree by selecting Clock \rightarrow Display \rightarrow Display Clock Tree.

10. Select Optimize → Optimize Design again Set the options as shown in the figure below.

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Design Stage		
O Pre-CTS	Post-CTS	Post-Route
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We selected Post-CTS this time. It means the optimization is performed after clock tree synthesis.

11. Select Route→NanoRoute→Route

Set the parameters and options as shown in the figure below.

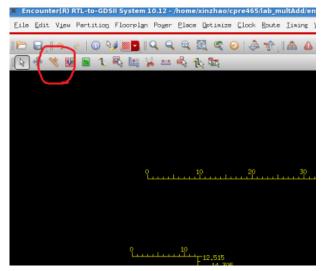
000	X NanoRoute
Routing Phase	
🗹 Global Route	
⊻ Detail Route	Start Iteration 0 End Iteration default
Post Route Optimi	zation 📃 Optimize Via 📃 Optimize Wire
Concurrent Rout	ing Features
🗹 Fix Antenna	🔄 Insert Diodes 🛛 Diode Cell Name
Timing Driven	Effort 5 Congestion Timing S.M.A.R.T.
SI Driven	
Post Route SI	SI Victim File 📄
🔲 Litho Driven	
🔲 Post Route Lith	io Repair
- Routing Control -	
Selected Nets	Only Bottom Layer default Top Layer default
ECO Route	
🔲 Area Route	Area Select Area and Route
Job Control	
🛃 Auto Stop	
Nu	imber of Local CPU(s): 1
Number of CUP(s)	per Remote Machine: 1
Number	of Remote Machine(s): 0
Set Multiple C	PU
	ny Attribute Mode Save Load Cancel Help

12. Select Optimize → Optimize Design

This time, we select Post-Route because we have already performed routing.



- 13. Now you have finished placement and routing.
 - To report power, type report_power.
 - To get area information, use the ruler which is circled by red below:



- To report worst timing path, type report_timing in the command window.
- To debug timing violations, select Timing→Debug Timing.
- To save your design, type "saveNetlist -excludeLeafCell design_pr.v" in the command window.
- To output RC parameters of your design, type "rcOut -spef design.spef" in the command window.
- To output .sdf (Standard Delay Format) file, select Timing→Write SDF. The .sdf file contains the information required for signal delay calculation. This file would be needed if we perform post layout simulation in ModelSim.