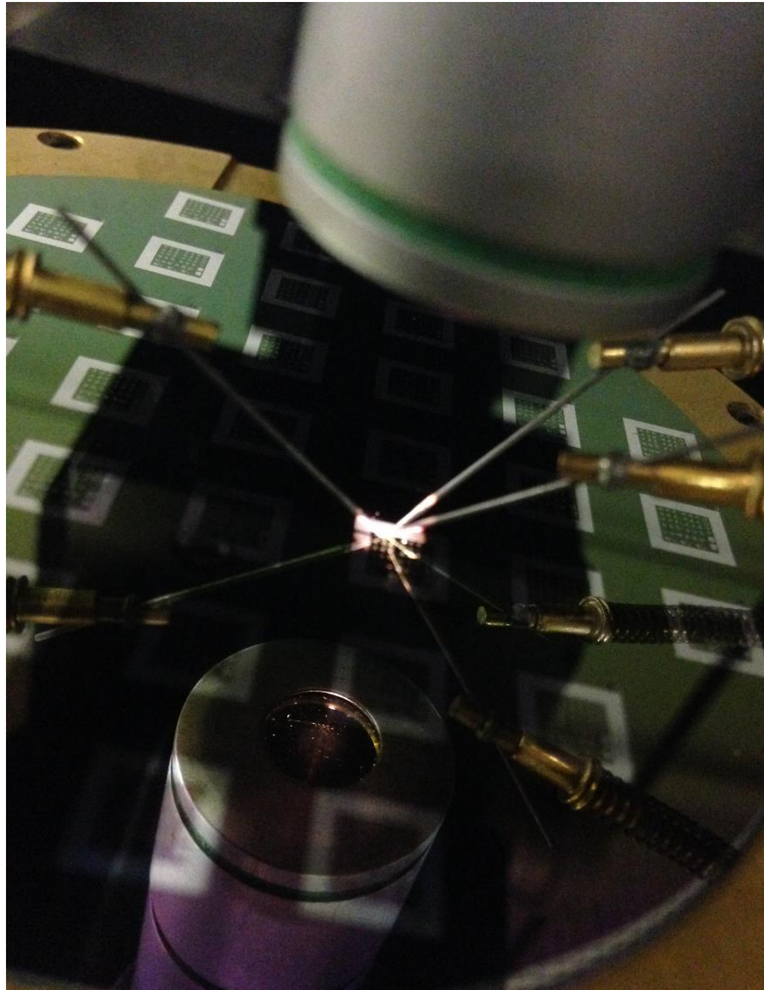
EE 432/532: Gate Pattern, Metallization, and Characterization CyMos process Final Report



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Overview

In this lab we finished our CyMos devices. We concluded the set of labs with use of self-aligning techniques for patterning out gate, a metallization process of depositing a layer of Aluminum for contacts, and finally characterization of the devices on the wafer through use of a 3 point probe. Unfortunately our lab process had run into some procedural errors not to our own fault with a layer of what we believe to be Aluminum Oxide left during the metallization process. In order to compensate for this we utilized a previously made device wafer to practice device characterization.

Patten for Gate

Wafer #	Oxide Thickness (nm)
1	239.9
2	241.0
3	238.9
4	236.9

The purpose of the gate lithography was to pattern the location and use the self-alignment technique to insure a properly working set of devices on our wafer. Not all of our device wafers had made it this far and we had only been left with four device wafers at this point with their corresponding thickness in the table above.

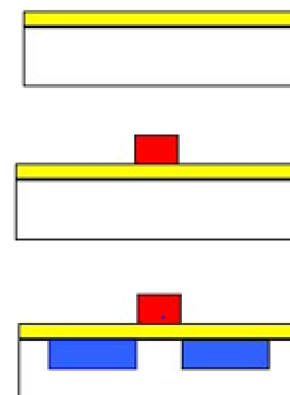


Figure 1- a step by step diagram of Self-Alignment technique

In order to correctly utilize this technique you need to first form the gate insulator in which we did. Then following that we had to form the gate of desired size and spacing that we desire through photolithography and then grow the gate. Once the gate has been formed we used a mask that

established the source and drain around the gate so they are automatically aligned precisely where they need to be and reduced any chance of gate overlay. Having any gate overlay would decrease the devices performance as well as if the gate did not connect the source and drain would not work.

Our photolithography process was the same minus the wet etching process. This time we utilized a dry oxidation process which is more precisely controlled although has the drawback of taking much longer than wet etching. Dry etching is easy to start and stop and is less sensitive to variables in its environment while wet etching is highly selective, causes no damage to the substrate, and in general is much cheaper. In our case we had the opportunity to use dry etching. We started with a standard clean of our wafers followed by a cleaning process of the quarts tube in our finance. In order to clean the tube we set the temperate to 800 degrees Celsius and set the ambient atmosphere to 1 slpm of dry Nitrogen gas. We then loaded our dry wafers onto the quartz boat that was stored within the furnace's tube. As before we placed the wafers in an order in which there are guard wafers on the outer edges to protect our device wafers form damage in processing. Pushing the boat into the center of the furnace at the rate of 1 inch every 12 seconds which in turn took a total of 5 mins. Once it was centered in the oven we stared the ramp up process for the next 10 mins to 1100 degree Celsius. Once the corrected temperature was reached we started the oxidation process. We started the oxygen flow at around 1 slpm and timed the process for 19 minutes and then reverted the oven back to a 0.3 flow of Nitrogen gas. The ramp process was then started to 800 degrees Celsius and required 30 minutes. We then unloaded the waves in a process akin to loading just in reverse.

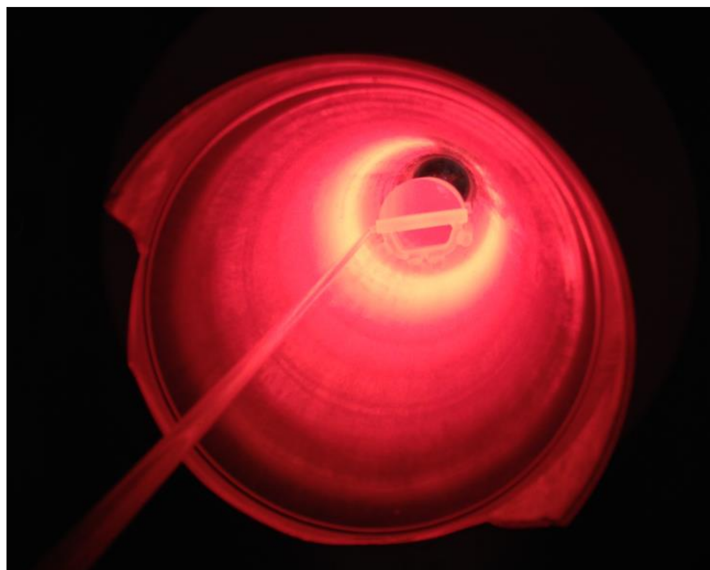


Figure 2- Dry etching process in quartz tube #3

Photolithography for contact vias

Once we needed to mask our 5th mask we realized all but 2 of our device wafers had been mis-aligned. The object was to use the same photolithography process as before on the previously applied layers but this time for the contact vias. In the figure to the right you can see an example of one of our correctly aligned device wafers. This was the step to prepare the wafer for metallization and apply the Aluminum contact areas which you can see on the left.

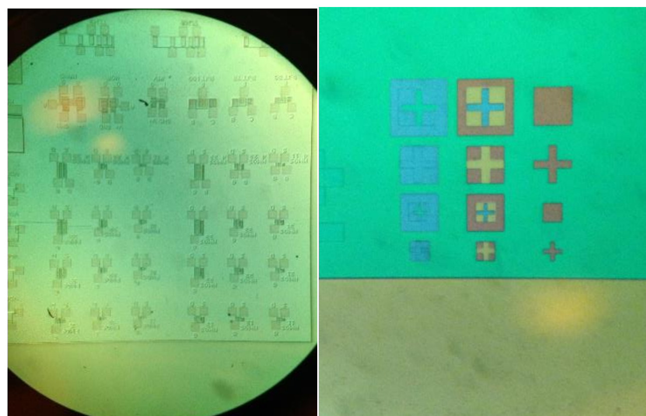


Figure 3- On the left you can see the completed contacts and on the right is an image of the alignment procedure up to the 5th mask

We started off with cleansing of our wafers as we do with every procedure. We then spun our wafers with the HMDS at 4000RPM for 25 seconds. Immediately following we spun the photo resist AZ5214-E at around 4000RPM for 40 seconds. We then utilized the same process as before in previous processes and prebaked the wafers on hot plates for 60 seconds at 120 degrees Celsius. We then aligned the mask and exposed each wafer individually for 70 seconds. Now we have to develop the photoresist that is left by gently agitating each Si wafer in MIF-300 developer for at least 60 seconds. Once the etching outline has been fully developed we moved the wafers to the cascade rinse for a minimum of 3 minutes then dried and inspected the outline under a microscope for quality control. Following inspection we did a quick soft post-bake at 120 degrees Celsius for 1 minute on hot plates again.

For the first etching of our contact vias we dipped the developed Si wafers in our BOE tub for precisely 2.5 minutes. We did 30 second intervals checking to see if the wafers had become hydrophilic or not. Once hydrophobic we knew they had been properly etched.

We then continued with a 2 minute cascade rinse followed up with a 3 minute bath in acetone. Once those 3 minutes were up we transferred the wafers to another acetone bath for 1 minute; followed by a 1 minute methanol bath and finally a 2 minute cascade rinse. To complete the process we put the wafers in the spin washer.

Metallization and Photolithography

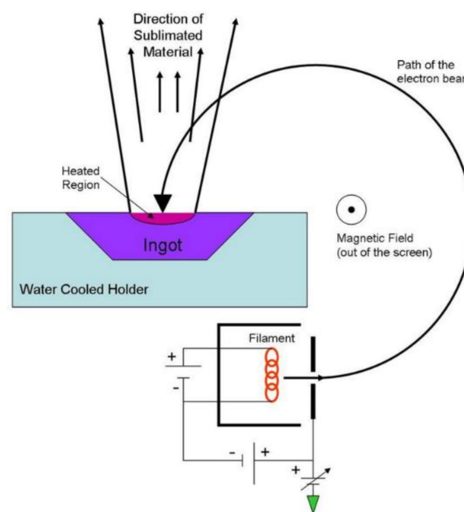


Figure 4- A diagram of Electron Beam Deposition

Once the patter had been laid for the contacts we had to deposit what would be the conducting material. Metallization is a process that connects individual devices together by a mean of microscopic wires, in our case our device contacts. In our case utilized an ion implantation device to deposit Aluminum on our device wafers. This deposition of Aluminum was done by electron beam vapor deposition. The general idea of the electron beam vapor deposition is the wafer acts as a target for the vaporized Aluminum to layer onto the wafer in a low temperature process. This process required an expensive setup and vacuum system. If there is not a vacuum present the impurities in the in the air will cause not just Aluminum to be deposited onto the wafer during the metallization process. Below the wafers is a source of Aluminum in this case which is vaporized with high voltage in which then flows onto the wafers placed in a circle. This process can be tightly controlled and is time consuming but results in a highly uniform distribution on Aluminum on the surface. Electron beam deposition is a form of physical vapor deposition which allows high control and low temperature processing unlike chemical vapor deposition processes which take place at high temperatures and a very high deposition rate around 0.1 micrometers a minute to 100 micrometers a minute. Unfortunately in our case, there was some malfunction in the vacuum process and left our original device wafers with a layer of Aluminum and Aluminum Oxide in which we could not remove later on by our normal Aluminum removing solution.

Annealing/sintering process

The annealing process was used in our case to repair in damaged substrate by the previous processing. Previous processes may have caused micro cracks and inconsistencies in the device wafer. The sintering process reduces the porosity/damaged we caused earlier by re-align the lattice structure. This in turn increases electrical conductivity, thermal conductivity, and as well as structural integrity of our device wafers. This is done by heating our wafers in an over at a high enough temperature in which the atoms can reform in the wafer while not reaching the melting point of the Aluminum that was previously deposited. If too high of a temperature is utilized you can create spikes of Aluminum which can ruin devices and nullify all the work previously done on the wafers as diagramed on the right. In industry they utilize heat lamps which can heat a wafer uniformly quickly and many wafers at a time in a process called rapid thermal processing. In our lab we do not have access to the correct equipment as in industry due to cost and utilized furnace annealing which warrants the same ending result in a matter of minutes in a more cost effective manner.

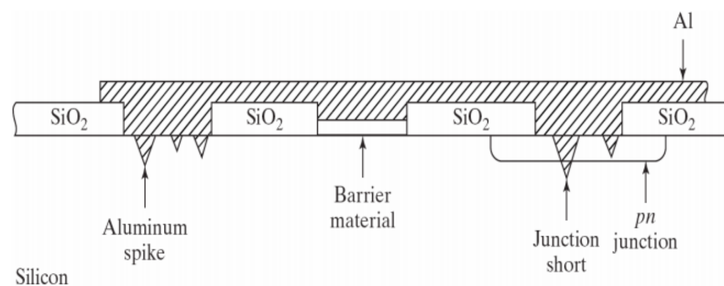


Figure 5-Digram of Aluminum "spiking" into silicon wafer

Testing Results

NMOS/ PMOS Transistors

$$I_D = \begin{cases} 0 & (V_{GS} \le V_T) \\ K[2(V_{GS}-V_T)V_{DS}-V_{DS}^2] & (V_{DS}<V_{GS}-V_T,\ V_{GS}>V_T) \\ K(V_{GS}-V_T)^2 & (V_{DS} \ge V_{GS}-V_T, V_{GS}>V_T) \end{cases}$$

$$K=\frac{1}{2}\mu C_{ox}\frac{W}{L}$$

Figure 6 - Breakdown of Ids

Where µ is the mobility of the carriers, Cox is the capacity of the oxide, W and L are the width and length of the channel respectively. If the drain voltage VDS is kept at a constant value higher than V -V GS T, the channel is "pinched off" because increases in VDS have no affect on ID. This saturation effect can be used to measure the threshold voltage governed by D GS T I = K (V -V). From the plot of the square-root of ID vs. VGS, K can be derived from the slope, and VT can be obtained from the interception with the VGS axis. The NMOS measurement is done in die 1 of our sintered wafer. The gate voltage sweeps from 0 to 5V in a step of 50mV, while the drain voltage is held constant at 8V. The detailed measurement result is illustrated in the tables below. The shaded data denote outliers, are therefore not included in the data averaging.

NMOS, 4-contact					NMOS, 3-contact				
#	Vt[V]	K[mA/V²]	W/L	µCox[mA/V²]	#	Vt[V]	K[mA/V²]	W/L	µCox[mA/V²]
1	N/A	N/A	2	N/A	9	N/A	N/A	2	N/A
2	1.41	6.605	4	3.302	10	1.64	9.9856	4	4.99
3	1.18	33.64	8	8.41	11	1.82	21.4369	8	5.36
4	N/A	N/A	2	N/A	12	1.19	5.4289	2	5.43
5	1.25	10.82	4	5.412	13	1.76	11.2896	4	5.64
6	0.63	4.04	8	1.01	14	1.41	20.9764	8	5.24
7	1.63	16.65	4	8.323	15	1.67	7.6729	4	3.84
8	0.66	4.537	2	4.537	16	-4.58	2.2801	2	2.28

Averaged Results for NMOS	
Vt[V]	µCox[mA/V2]
1.496	5.5947

Figure 7- Charts showing NMOS results

The PMOS measurement is also done in die 1 of our sintered wafer. The gate voltage sweeps from - 5V to 0V in a step of 50mV, while the drain voltage is held constant at -8V. The detailed measurement result is illustrated in the tables below. The shaded data denote outliers, are therefore not included in the data averaging.

PMOS, 4-contact					PMOS, 3-contact				
#	Vt[V]	K[mA/V^2]	W/L	C_{ox}[mA/V^2]	#	Vt[V]	K[mA/V^2]	W/L	C_{ox}[mA/V^2]
1	N/A	N/A	2	N/A	9	N/A	N/A	2	N/A
2	N/A	N/A	4	N/A	10	0.4	18.836	4	9.4
3	0.3	40.7044	8	10.2	11	-0.6	61.937	8	15
4	-2	13.2496	2	13.2	12	N/A	N/A	2	N/A
5	-1	31.2481	4	15.6	13	-1.4	26.626	4	13
6	-1	54.9081	8	13.7	14	-1.6	45.833	8	11
7	-2	20.3401	4	10.2	15	-1.6	19.097	4	9.5
8	-2	10.7584	2	10.8	16	-1.5	11.424	2	11

Averaged Results for PMOS	
Vt[V]	µCox[mA/V2]
-1.567	12

Figure 8- Results of PMOS

I-V Curves for NMOS/PMOS Transistors We tried to record a set of ID vs. VDS curves (use at least five values of VG beyond the threshold voltage) and the corresponding square-root of ID vs. VGS, curves for at least three PMOS and three NMOS (say, one each of the 5-, 10-, and 20-micron length gates). But it is found that for both PMOS and NMOS, the small device does not work at all. And then when we tried to dump the data files from the floppy disk, some of them have already been damaged. So only some of our results are illustrated below on the following page.

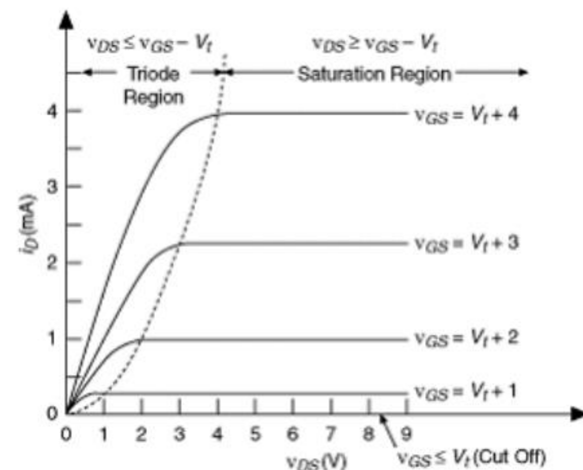
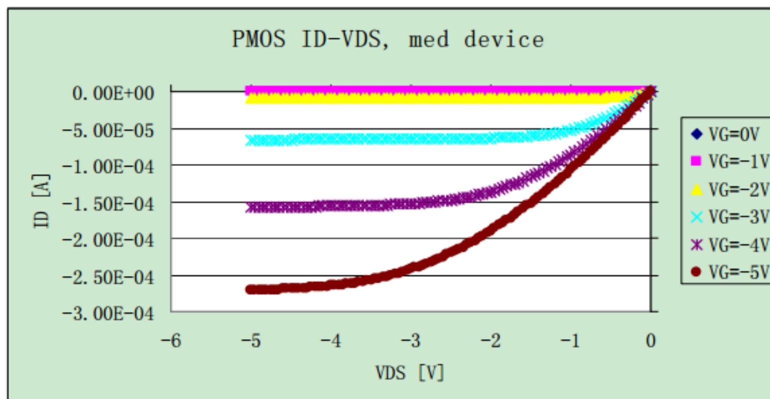
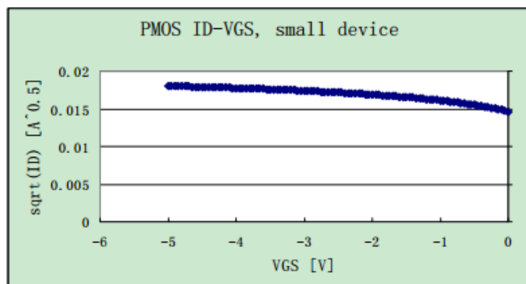


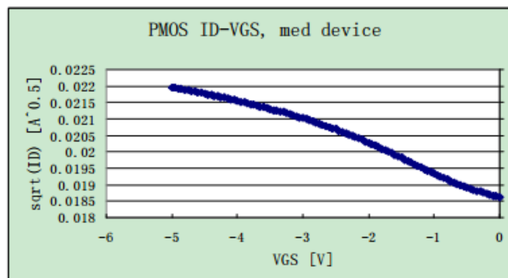
Figure 9- I-V damily for the NMOS transistor

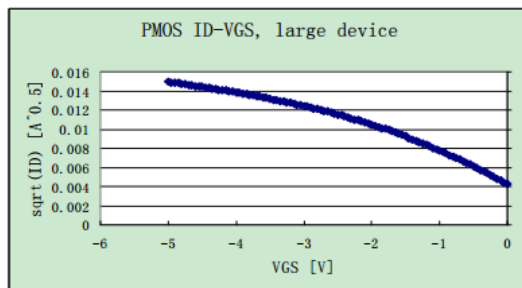
I-V curves of NMOS transistors

The I-V characteristic curves we obtained are almost the same as the above schematic diagram. In our case, the small NMOS device does not function well. The data for the med NMOS device is damaged, and can not be dumped out from the floppy disk. The only results we have for the large NMOS device seem not be a good example, and so are not drawn here.









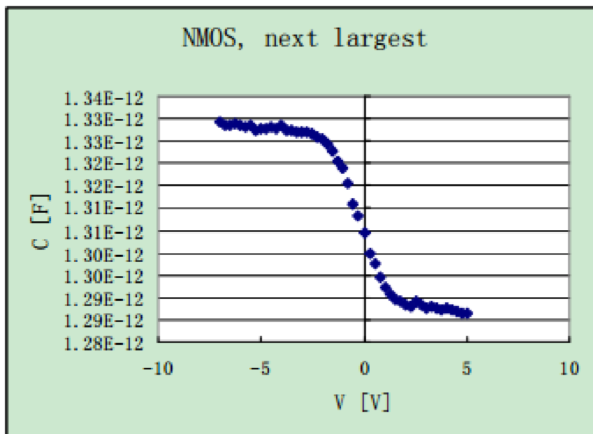
Generally speaking, the small transistors (with small dimensions around 5 µm) do not work well. This may be due to a combination of effects from undercutting, lateral diffusion, mask alignment and so on. The oddity we found with the N/PMOS testing is that the plot of the square-root of ID vs. VGS does not start from zero current though we increase the gate voltage from 0. This implies that there may be other

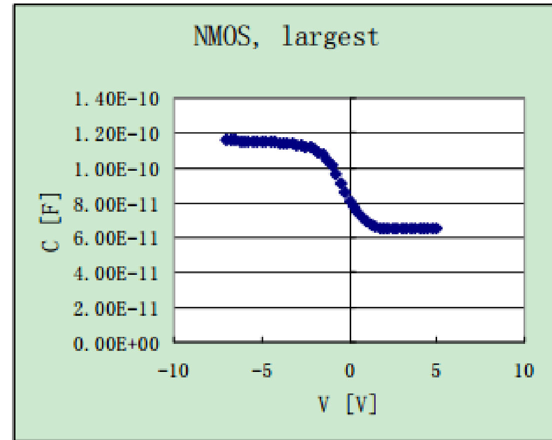
parallel path of current. Also, rather than a clear cut on the gate voltage axis, the curve gets round near the interception with the gate voltage axis. This may also be associated with the potential parallel current path mentioned earlier. In addition, the ID~ VDS curve family looks weird near the origin.

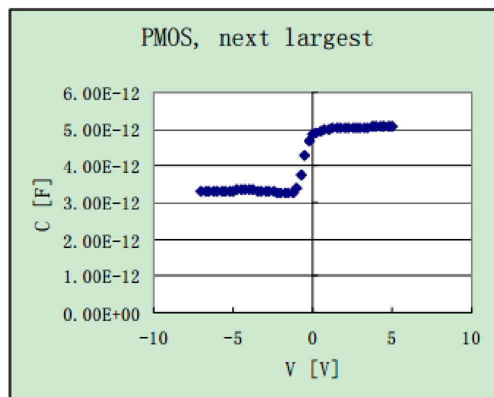
For some MOSFETs the plot of the square-root of ID is sublinear (meaning that it is not a straight line, but bends down at higher gate voltages). This is an indicator that the simple model for the MOSFET will probably not provide a very good description of the real MOSFET's behavior. When trying to find the threshold voltage for a MOSFET that displays this type of behavior, we tried to fit the straight line at lower gate voltages - just slightly above threshold. Otherwise, if we use higher gate voltages - in the region where the curve is bending - the extracted threshold voltage will be unreasonably low and perhaps even negative.

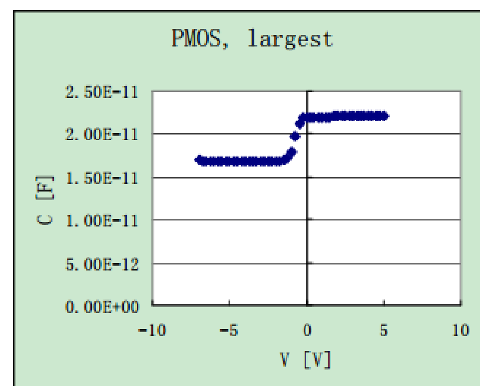
MOS Capacitors

We used the C-V meter to measure the capacitance of the NMOS and PMOS capacitor structure. The bias voltages is given in the range of -7~5 V in .25 step. The oxide capacitance Cox is the maximum value measured. Note that Cox is measured in units of F/cm2.









	NMOS, next largest	NMOS, largest	PMOS, next largest	PMOS, largest
C [F]	1.33E-12	1.16E-10	5.07E-12	2.21E-11
A_{ox} [cm^2]	4 E-4	1.6 E-3	4 E-4	1.6 E-3
C_{ox} [F/cm^2]	3.325 E-9	7.25 E-8	1.2675 E-8	1.38125 E-8

The averaged value of Cox is 2.5578×10-8 F/cm2.From the definition of capacitance, we have to the right.The relative static permittivity (sometimes called the dielectric constant) εr of silicon dioxide is 3.9, and the electric constant ε0 is ~8.854×10−12 F m−1. Then, we have εox=εrε0=3.45306×10−11 F m−1.

$$C=\frac{\varepsilon_{ox}A_{ox}}{t_{ox}},\quad C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$$

Figure 10 - Capacitance Equation Note that Cox is measured in units of F/cm2. This means that A is fixed to be one square centimeter

Finally, the oxide thickness can be determined by the following equation:

$$t_{ox}=\frac{\varepsilon_{ox}}{C_{ox}}=\frac{3.45306\times10^{-9}\,Fcm^{-1}}{2.5578\times10^{-8}\,Fcm^{-2}}=0.135\text{cm}=1.35\text{mm}$$

Figure 11- Ox thickness calculation

The calculated oxide thickness is several orders of magnitude larger than the expected value 40nm.

Conclusion

Over the semester we have learned many fabrication techniques in creation of our CyMos device. The final result unfortunate was something we could not account for by being ruined in one of the final stages of the processes (Metallization). This was a good lesson on how sensitive the fabrication process is to small variables. Although the lab did not end with a working device wafer, we did learn the fabrication process and have all been enriched by it and have been instilled with the confidence to take these process and apply them in industry/practice.